CALL 2011-2

Project profile

EPT300

Enabling power technologies on 300mm wafers

The volume manufacturing benefits of 300 mm silicon wafer fabrication are well-established with regard to digital integrated circuits but the ability to use them in the production of power semiconductor devices has so far eluded large-scale producers. The ENIAC JU project EPT300 aims to develop and implement technology to achieve full-scale production of power devices on 300 mm wafers. This will place European fabs at the forefront of power semiconductor manufacturing worldwide and open up further employment opportunities both in the fabs and across the entire European electronics industry.

Sub Programme

- Equipment, materials and manufacturing for nanoelectronics

Major elements of the European Commission's Europe 2020 strategy are the reduction of greenhouse gas emissions, energy efficiency and electro-mobility. A key enabler to realise these goals will be the production of power semiconductors designed and manufactured at low cost and in sufficient quantities in Europe with equipment and materials supplied by European companies.

The ENIAC JU project EPT300 will be a decisive step forward in the strengthening of Europe's leading position in power semiconductor technologies and 'More-than-Moore' manufacturing capabilities. The fabrication of power semiconductor devices on 300 mm wafers in a leading European pilot line will require manufacturing excellence, cost competitiveness and challenging applications.

ETP300 plans to realise demonstrators on a pilot production line and to prove the readiness for large-scale manufacture in a fabrication environment based on selected products and technologies.

Power device complexity

Power semiconductor production is highly complex and involves many stages requiring in-depth materials knowledge and expertise. A first precondition is the availability of the proper raw materials and production equipment. The initial manufacturing stages deal with semiconductor front-end processing comprising a series of steps in which the active area of the device is built up.

Subsequent stages deal with semiconductor back-end production. These include thin-layer metallisation and a set of particular active wafer back-end process steps, which are essential in the manufacture of power semiconductors. One key process is wafer thinning, since the thickness of a power device has considerable influence on its performance. Further manufacturing steps include device testing and device assembly.

EPT300 intends to:

1. Enhance the core competences of European companies in the development of technology for power

semiconductors and the ability to manufacture at competitive cost in Europe;

2. Achieve best-in-class productivity in the fabrication of leading-edge power semiconductors while addressing advanced, energy-efficient applications for industrial and mobility purposes; and
3. Develop the supply chain for the manufacture of leading-edge power semiconductor technologies in Europe.

Fabrication challenges

The project will address challenges on process technologies, production technologies and the handling and automation of advanced power technologies based on 300 mm wafers. Developments will include:

- Wafer substrate materials for 300 mm diameter thin wafers in power applications;
- New process capabilities and approaches aimed at resolving the absence of suitable substrate materials;
- Enabling of processing equipment with capabilities derived from the requirements of manufacturing power devices on thin 300 mm wafers;
- Safety requirements for new process technologies and statistical methods for lifetime assessments for advanced power technologies based on 300 mm wafers;
- Advanced multi-parameter simulation methods and models for in-depth systems investigation, prediction and optimisation;
- Handling and automation concepts for thin wafer and special requirements of More-than-Moore fabrication lines;
- Co-existence strategies for integrated multi-diameter wafer manufacturing; and
- Application requirements for demonstrators and corresponding quality requirement profiles.

A primary objective is to conduct research into, so far unexplored, technological capabilities for setting up in the future a networked fully-integrated pilot line for the fabrication of power semiconductors on 300 mm wafers. Once completed, the outcome of the work will be demonstrated for fully functional metal oxide on silicon field-effect transistor and insulated gate bipolar transistor products manufactured in Europe, proving both functionality and reliability in the application environment. Readiness for implementation in high volume production will be demonstrated by the end of the project.

European/global benefits

With the help of this ENIAC JU project, European semiconductor manufacturing and the European equipment and materials industries will be first in the world with a 300 mm power semiconductor processing line dedicated to power-device production. EPT300 therefore represents a major step forward in the realisation of leading-edge manufacturing capabilities in Europe.

As a consequence, significant employment opportunities are expected to result both in the fabs and for those European companies likely to make use of the new power semiconductor technologies resulting from this project.

Equipment, materials and manufacturing

Partners:

- Artesyn Austria
- ASM Europe
- Bruco Integrated Circuits
- CTR Carinthian Tech Research
- Eutema Technology Management
- HAP Handhabungs-, Automatisierung- und Präzisionstechnik
- Heliox
- Infineon Technologies
- LAM Research
- LPE
- Mechatronic Systemtechnik
- Philips Medical Systems
- Prodrive
- Roth & Rau - Ortner
- Semikron Elektronik
- SICO Technology
- Siltronic
- Technical University of Dresden
- Technical University of Eindhoven
- University of Klagenfurt

Project co-ordinator:

- Johann Massoner, Infineon Technologies

Key project dates:

- Start: April 2012
- Finish: March 2015

Countries involved:

- Austria
- Germany
- Italy
- The Netherlands

Total budget:

- €43.65 million

The ENIAC Joint Undertaking, set up in February 2008, co-ordinates European nanoelectronics research activities through competitive calls for proposals. It takes public-private partnerships to the next level, bringing together the ENIAC member states, the European Commission and AENEAS, the association of R&D actors in this field, to foster growth and reinforce sustainable European competitiveness.

Details correct at time of print but subject to possible change. Updates will be included in the project summary at the end of the project.

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