

Senate

Seven Nanometer Technology

ASML

The SeNaTe project is the next in a chain of thematically connected ENIAC JU KET pilot line projects which are associated with 450mm/300mm development for the 12nm and 10nm technology nodes. The main objective of the SeNaTe project will be the demonstration of the first 7nm IC technology integration in line with the ITRS roadmap on real devices in the Advanced Patterning Center at imec using innovative device architecture and comprising demonstration of a complete holistic lithographic platform for EUV and immersion technology, advanced process and metrology platforms, new materials and mask infrastructure.

Lithography scanners will be developed based on 193nm immersion and on EUV technology to achieve the 7nm module patterning specification. Metrology platforms need to be qualified for N7's 1D, 2D and 3D geometries with the appropriate precision and accuracy. For the 7nm technology modules a large number of new materials will need to be introduced. The introduction of these new materials brings challenges for all involved processes and the related equipment set. Next to new deposition processes also the interaction of the involved materials with subsequent etch, clean and planarization steps will be studied. Major European stakeholders in EUV mask development will collaboratively work together on a number of key remaining EUV mask issues.