

Waytogo

Which Architecture Yields Two Other Generations Of CMOS

STMicroelectronics

The proposed pilot line project WAYTOGO CMOS objective is to keep Europe in the race for leading edge digital CMOS technologies at node 10nm and prepare following node transistor architecture. Capitalizing on the dynamic created by the introduction of the 28nm FDSOI (Fully Depleted transistors built on Silicon On Insulator) technology the project would like to enlarge the FDSOI ecosystem by:

- enhancing the 14FDSOI design platform capabilities, particularly in low power design;
- -offering an optimized Power-Performance-Area-Cost (PPAC) trade-off for a Node10 CMOS technology platform built on SOI substrate;
- -researching architectural options to evolve FD devices into the next node (beyond 10nm).

Keeping the design activities in close collaboration with the technology definition will help tailor the PPAC trade-off of the 10nm technology to the applications needs. The consortium is targeting to define the standard in term of leading edge energy efficient CMOS technology for a wide range of applications battery operated or not.

To reach the objective of installing a pilot line capable of prototyping CMOS integrated circuits at 10nm in Europe the consortium gather a large group of partners across the semiconductor value chain: academics/institutes, equipment and material providers, semiconductor companies, EDA providers, IP providers, fabless design houses.